AP-754

APPLICATION NOTE

Migrating from the 8XC196KB16 to the 8XC196KC20

March 1997

Order Number: 273013-001

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1.0 INTRODUCTION

Both the 8XC196KB and 8XC196KC microcontrollers are high performance members of the MCS® 96 family, which is designed to handle high speed input output (HSIO) operations. Though they share a common architecture and instruction set, there are a few design considerations involved when migrating from the 8XC196KB to the 8XC196KC.

This application note describes enhancements and outlines differences to help the user migrate 8*X*C196KB designs to the 8XC196KC. Consult the *8XC196KB Microcontroller User's Manual* (order number 270651), the *8XC196KB 16-bit High Performance Microcontroller* datasheet (order number 270909) for specifications, and the *8XC196KC/8XC196KD Microcontroller User's Manual* for in-depth descriptions and specifications.

2.0 ARCHITECTURAL DIFFERENCES

This section lists the main features of the 8XC196KB and 8XC196KC for comparison. The major differences of the 8XC196KC from the 8XC196KB:

- pinout considerations
- memory size
- operating frequency
- peripherals
- address map

2.1 Address Space, Speed, and Peripherals Differences

The 8XC196KC is an enhanced version of the 8XC196KB microcontroller, having more address space, operating at a higher frequency, and supporting new peripheral designs. Table 1 lists all the enhancements of the 8XC196KC with respect to the 8XC196KB.

Table 1. Feature Comparison

Feature	8XC196KB	8XC196KC
ROM	8K bytes	16K bytes
Frequency	16 MHz	20 MHz
Register RAM	256 bytes	512 bytes
PWM	1 channel	3 channels
A/D	10-bit	8- and 10-bit
Interrupt	Standard	PTS

2.2 Pinout Differences

The 8XC196KB and 8XC196KC are pin compatible with the exception of several pins that have different multiplexed functions. Table 2 highlights those pins.

Table 2. Multiplexed Pin Assignment Differences Between the 8XC196KB and 8XC196KC

Multiplexed Function Difference	8XC196KB	8XC196KC
Pulsewidth Modulator Output	P1.3	P1.3 / PWM1
Pulsewidth Modulator Output	P1.4	P1.4 / PWM2
Slave Identification Number	HSI.0 / SID.0	HSI.0
Slave Identification Number	HSI.1 / SID.1	HSI.1
Slave Identification Number	HSI.2 / HSO.4 / SID.2	HSI.2 / HSO.4
External Interrupt	ACH7 / P0.7 / PMODE.3	ACH7 / P0.7 / PMODE.3 / EXTINT
Slave Identification Number	HSI.3 / HSO.5 / SID.3	HSI.3 / HSO.5
Cumulative Program Verify	P2.6 / T2UP–DN	P2.6 / T2UP–DN
Pulsewidth Modulator Output	P2.5 / PWM	P2.5 / PWM0

Table 2 shows that the slave identification number (SID.*x*) pins, which were used on the 8XC196KB to assign each slave controller a pin of Port 3 or Port 4 for passing program verification data, are omitted from the 8XC196KC pinout.

Enhancements to the 8XC196KC pinout, when compared to the 8XC196KB, include:

- 3 pulsewidth modulator (PWM) output pins, instead of 1 PWM output pin.
- 2 external interrupt (EXTINT) input pins, instead of 1 EXTINT pin.
- 1 cumulative program verification (CPVER) output pin.

2.3 Address Map Differences

As a direct result of the additional on-chip ROM, register RAM, and redesigned interrupt structure; there exist some differences between the address maps of the 8XC196KB and 8XC196KC. Table 3 details the differences.

Table 3. Address Map Differences Between the 8XC196KB and 8XC196KC

Description	8XC196KB	8XC196KC
External memory or I/O	4000 – FFFFH	6000 – FFFFH
Internal nonvolatile or external memory	2080 – 3FFFH	2080 – 5FFFH
Reserved (write FFH)	2040 – 207FH	205E – 207FH
PTS vectors	—	2040 – 205DH
Upper interrupt vectors	2030 – 203FH	2030 – 203FH
ROM security key	2020 – 202FH	2020 – 202FH
Reserved (write FFH)	201A – 201FH	201A – 201FH

Table 3. Address Map Differences Between the 8XC196KB and 8XC196KC (Continued)

Description	8XC196KB	8XC196KC
Reserved (write 20H)	2019H	2019H
Chip configuration byte (CCB)	2018H	2018H
Reserved (write FFH)	2014 – 2017H	2014 – 2017H
Lower interrupt vectors	2000 – 2013H	2000 – 2013H
Ports 3 and 4	1FFE –1FFFH	1FFE –1FFFH
External memory	0100 – 1FFDH	0200 – 1FFDH
Register RAM	0018 – 00FFH	0018 – 01FFH
CPU SFRs	0000 – 0017H	0000 – 0017H

2.4 Windowing Differences

As with the 8XC196KB microcontroller, the 8XC196KC uses a horizontal windowing scheme that switches a 24-byte memory block within the lowest 24 bytes of the lower register file. Unlike the 8XC196KB, which uses two horizontal windows (HWindow 0 and HWindow 15), the 8XC196KC uses three horizontal windows (HWindow 0, HWindow 1, and HWindow 15). Each HWindow provides read and write access to a unique combination of SFRs. A particular HWindow is selected by writing the desired HWindow number into the Window Select Register (WSR, 14H). Table 4 lists the twelve registers in HWindow 1 that are available only on the 8XC196KC.

Table 4. Horizontal Window 1 (HWindow 1)

Address (Hex)	SFR
17	PWM2_CONTROL
16	PWM1_CONTROL
15	Reserved
14	WSR
13	INT_MASK1
12	INT_PEND1
11	Reserved
10	Reserved
0F	Reserved
0E	Reserved
0D	Reserved
0C	IOC3
0B	Reserved
0A	Reserved
09	INT_MASK
08	INT_PEND
07	PTSSRV (H)

Table 4. Horizontal Window 1 (HWindow 1) (Continued)

Address (Hex)	SFR
06	PTSSRV (L)
05	PTSSEL (H)
04	PTSSEL (L)
03	AD_TIME
02	Reserved
01	ZERO_REG (H)
00	ZERO_REG (L)

2.5 Register Differences

With the introduction of new features like the programmable 8-bit and 10-bit A/D converter with programmable sampling and conversion times, there have been changes made to some of the register bit definitions, as well as, the addition of some new registers.

On the 8XC196KC, the input/output control 2 (IOC2) register has been modified. In Figure 1, the **bold** bit mnemonic indicates a new bit definition that is a reserved bit location on the 8XC196KB.

IOC2

Address: 0BH
Reset State: 00H

The input/output control 2 (IOC2) register controls three Timer 2 options, the clock prescalers for the PWM and the A/D converter, and the source for A/D conversion time determination. IOC2 also enables and disables locking commands into the HSO CAM, and it can clear all entries from the HSO CAM.

7							0
CAM_CLR	LOCK_ENA	T2ALT_INT	AD_FAST	**AD_TIME_ENA**	SLOW_PWM	T2UD_ENA	FAST_T2_ENA

Bit Number	Bit Mnemonic	Function
7	CAM_CLR	Clear All Content-addressable Memory (CAM) Entries Setting this bit clears all entries (including locked entries) from the HSO CAM. This bit is not latched; it will always read as “1” in HWindow 15.
6	LOCK_ENA	Enable Locked CAM Entries This bit enables and diables command locking. When this bit is set, HSO_COMMAND.7 controls whether individual commands are locked into the CAM or cleared after execution. 0 = disable command locking 1 = enable command locking

Figure 1. Input/Output Control 2 (IOC2) Register

IOC2

Address: 0BH
Reset State: 00H

The input/output control 2 (IOC2) register controls three Timer 2 options, the clock prescalers for the PWM and the A/D converter, and the source for A/D conversion time determination. IOC2 also enables and disables locking commands into the HSO CAM, and it can clear all entries from the HSO CAM.

7							0
CAM_CLR	LOCK_ENA	T2ALT_INT	AD_FAST	**AD_TIME_ENA**	SLOW_PWM	T2UD_ENA	FAST_T2_ENA

Bit Number	Bit Mnemonic	Function
5	T2ALT_INT	Select Timer 2 Overflow Boundary This bit selects the overflow boundary for the Timer 2 Overflow interrupt (INT12, 2038H). INT_MASK1.4 must be set to enable the interrupt. 0 = FFFFH/0000H boundary 1 = 7FFFH/8000H boundary
4	AD_FAST	Disable A/D Clock Prescaler In 80C196KB-compatible mode (IOC2.3 cleared), this bit controls the A/D conversion time period by enabling or disabling the A/D clock prescaler (divided-by-two). If IOC2.3 is set, this bit is ignored. 0 = enable; conversion time is 156.5 state times, 80C196KB fast mode 1 = disable; conversion time is 89.5 state times, 80C196KB normal mode
3	**AD_TIME_ENA**	Enable AD_TIME Register This bit selects whether the A/D conversion times are controlled by the AD_TIME register or by the fast and normal conversion modes of the 80C196KB. When this bit is clear, IOC2.4 enables or disables the A/D clock prescaler for complete 80C196KB compatibility. 0 = 80C196KB-compatible mode 1 = AD_TIME register
2	SLOW_PWM	Enable PWM Clock Prescaler This bit controls the PWM output period by enabling or disabling a clock prescaler (divide-by-two) on PWM1, PWM2, and PWM3. 0 = disable; PWM output period is 256 state times 1 = enable; PWM output period is 512 state times

Figure 1. Input/Output Control 2 (IOC2) Register (Continued)

IOC2

Address: 0BH
Reset State: 00H

The input/output control 2 (IOC2) register controls three Timer 2 options, the clock prescalers for the PWM and the A/D converter, and the source for A/D conversion time determination. IOC2 also enables and disables locking commands into the HSO CAM, and it can clear all entries from the HSO CAM.

7							0
CAM_CLR	LOCK_ENA	T2ALT_INT	AD_FAST	**AD_TIME _ENA**	SLOW_PWM	T2UD_ENA	FAST_T2 _ENA

Bit Number	Bit Mnemonic	Function
1	T2UD_ENA	Enable Timer 2 Up/Down Count This bit controls whether Timer 2 functions as an up counter or as an up/down counter. 0 = count up only 1 = if P2.6 = 0, count up if P2.6 = 1, count down
0	FAST_T2_ENA	Enable Timer 2 Fast Increment This bit controls whether Timer 2 operates in fast increment or normal mode. When fast increment mode is enabled, the microcontroller does not use Timer 2 as the HSO reference and does not reset Timer 2. 0 = normal mode; count every eight states 1 = fast increment mode; count every state

Figure 1. Input/Output Control 2 (IOC2) Register (Continued)

The input/output control 3 (IOC3) register is new to the 8XC196KC and does not exist on the 8XC196KB. The IOC3 register selects either an internal or external clock source for Timer 2 (see Figure 2).

IOC3

Address: 0CH
Reset State: F0H

The input/output control 3 (IOC3) register selects either an internal or an external clock source for Timer 2 and selects the function of pin P1.3 and pin P1.4.

7							0
—	—	—	—	PWM2_SEL	PWM1_SEL	CLOCKOUT_DIS	T2_ENA

Bit Number	Bit Mnemonic	Function
7:4	—	Reserved; for compatibility with future devices, write zeros to these bits.
3	PWM2_SEL	PWM2 Select This bit selects the P1.4 pin function. 0 = PWM2 output 1 = quasi-bidirectional port pin
2	PWM1_SEL	PWM1 Select This bit selects the P1.3 pin function. 0 = PWM1 output 1 = quasi-bidirectional port pin
1	CLOCKOUT_DIS	CLKOUT Disable This bit reduces the noise in systems that do not require the CLKOUT signal. The actual value of the bit will read back in HWindow 1. 0 = enable CLKOUT 1 = disable CLKOUT
0	T2_ENA	Timer 2 Internal Clock Enable This bit controls whether Timer 2 is clocked internally or externally. 0 = external source: if IOC0.7 = 0, T2CLK (P2.3) if IOC0.7 = 1, HSI.1 1 = internal source

Figure 2. Input/Output Control 3 (IOC3) Register

On the 8XC196KC, the A/D command (AD_COMMAND) register has been modified. In Figure 3, the **bold** bit mnemonic indicates a new bit definition that previously had been a reserved bit location on the 8XC196KB.

AD_COMMAND

Address: 02H
Reset State: XXH

The A/D command (AD_COMMAND) register selects the A/D channel number to be converted, controls whether the A/D converter starts immediately or with an HSO command, and selects either 8-bit or 10-bit conversion mode.

7							0
—	—	—	**AD_MODE**	GO	ACH2	ACH1	ACH0

Bit Number	Bit Mnemonic	Function
7:5	—	Reserved; for compatibility with future devices, write zeros to these bits.
4	**AD_MODE**	A/D Conversion Mode This bit determines whether the microcontroller performs an 8-bit or a 10-bit conversion. 0 = 10-bit conversion 1 = 8-bit conversion
3	GO	A/D Conversion Trigger Writing this bit activates the A/D converter. The value that you write to it determines at what point a conversion is to start. 0 = HSO initiates conversion 1 = start immediately
2:0	ACH2:0	A/D Channel Selection These three bits select the channel number for conversion. **ACH2 ACH1 ACH0 Channel** 0 0 0 ACH0 0 0 1 ACH1 0 1 0 ACH2 0 1 1 ACH3 1 0 0 ACH4 1 0 1 ACH5 1 1 0 ACH6 1 1 1 ACH7

Figure 3. A/D Command (AD_COMMAND) Register

On the 8XC196KC, the A/D result (AD_RESULT) register has been modified. In Figure 4, the **bold** bit mnemonic indicates a new bit definition that previously had been a reserved bit location on the 8XC196KB.

AD_RESULT
HWindow 0 (Read)
HWindow 15 (Write)

Address: 03H
02H
Reset State: FEC0H

The A/D result (AD_RESULT) register consists of two bytes. The high byte contains the eight most-significant bits from the A/D converter. The low byte contains the two least-significant bits from a 10-bit A/D conversion, indicates the A/D channel number that was used for the conversion, and indicates whether a conversion is currently in progress.

15							**8**
AD_HI (Upper Nibble)				AD_HI (Lower Nibble)			
7							**0**
ADRLT1	ADRLT0	—	**MODE_ST**	STATUS	ACH2	ACH1	ACH0

Bit Number	Bit Mnemonic	Function
15:8	AD_HI	A/D High Result These bits contain the 8 most-significant bits of an A/D conversion result.
7	ADRLT1	A/D Result Bit 1 Bit 1 of a 10-bit A/D conversion result.
6	ADRLT0	A/D Result Bit 0 Bit 0 of a 10-bit A/D conversion result.
5	—	Reserved. This bit is undefined.
4	**MODE_ST**	A/D Conversion Mode Status Indicates whether this is an 8-bit or a 10-bit conversion. 0 = 10-bit conversion 1 = 8-bit conversion
3	STATUS	A/D Status Indicates the status of the A/D converter. Up to 8 state times are required to set this bit following a start command. When testing this bit, wait at least the 8 state times. 0 = A/D is idle 1 = A/D conversion is in progress
2:0	ACH2:0	A/D Channel Number These bits indicate the A/D channel number that was used for the conversion.

Figure 4. A/D Result (AD_RESULT) Register

The A/D time (AD_TIME) register is new to the 8XC196KC and did not exist on the 8XC196KB. This register programs the sample and conversion times for the A/D converter (see Figure 5).

AD_TIME

Address: 03H
Reset State: FFH

The A/D time (AD_TIME) register programs the sample window time and the conversion time for each bit. This register programs the speed at which the A/D can run — not the speed at which it can convert correctly. Consult the data sheet for recommended values. Initialize the AD_TIME register before initializing the AD_COMMAND register. Do not write to this register while a conversion is in progress; the results are unpredictable.

7							0
SAM2	SAM1	SAM0	CONV4	CONV3	CONV2	CONV1	CONV0

Bit Number	Bit Mnemonic	Function
7:5	SAM2:0	A/D Sample Time These bits specify the sample time. Use the following formula to compute the sample time. $SAM = \frac{T_{SAM} \times F_{OSC} - 2}{8}$ where: SAM = 1 to 7 T_{SAM} = the sample time, in µsec, from the data sheet F_{OSC} = the input frequency on XTAL1, in MHz
4:0	CONV4:0	A/D Bit Conversion Time These bits specify the conversion time for each bit. Use the following formula to compute the conversion time. $CONV = \left[\frac{T_{CONV} \times F_{OSC} - 3}{2 \times B}\right] - 1$ where: CONV = 2 to 31 T_{CONV} = the conversion time, in µsec, from the data sheet F_{OSC} = the input frequency on XTAL1, in MHz B = the number of bits to be converted (8 or 10)

Figure 5. A/D Time (AD_TIME) Register

2.6 Power Consumption Differences

Table 5 shows a comparison of four current consumption parameters for the 8XC196KB and 8XC196KC. For further details on the DC characteristics, refer to the latest revision of the 8XC196KB and 8XC196KC datasheets.

Table 5. Power Consumption Differences Between the 8XC196KB and 8XC196KC

Symbol	Parameter	8XC196KB (typical / maximum)	8XC196KC (typical / maximum)
I_{CC}	Active mode current in reset	50 / 60 mA	80 / 92 mA
I_{IDLE}	Idle mode current	10 / 25 mA	21 / 30 mA
I_{PD}	Powerdown mode current	5 / 30 mA	8 / 15 mA
I_{REF}	A/D reference supply current	2 / 5 mA	2 / 5 mA

3.0 PERIPHERAL CONSIDERATIONS

This section describes enhancements made to the 8XC196KC microcontroller's PWM peripheral, interrupt structure, slave programming routine, and Timer 2 clock.

3.1 Pulse-Width Modulator

Figure 6 shows a block diagram of the 8XC196KC pulse-width modulator (PWM) peripheral.

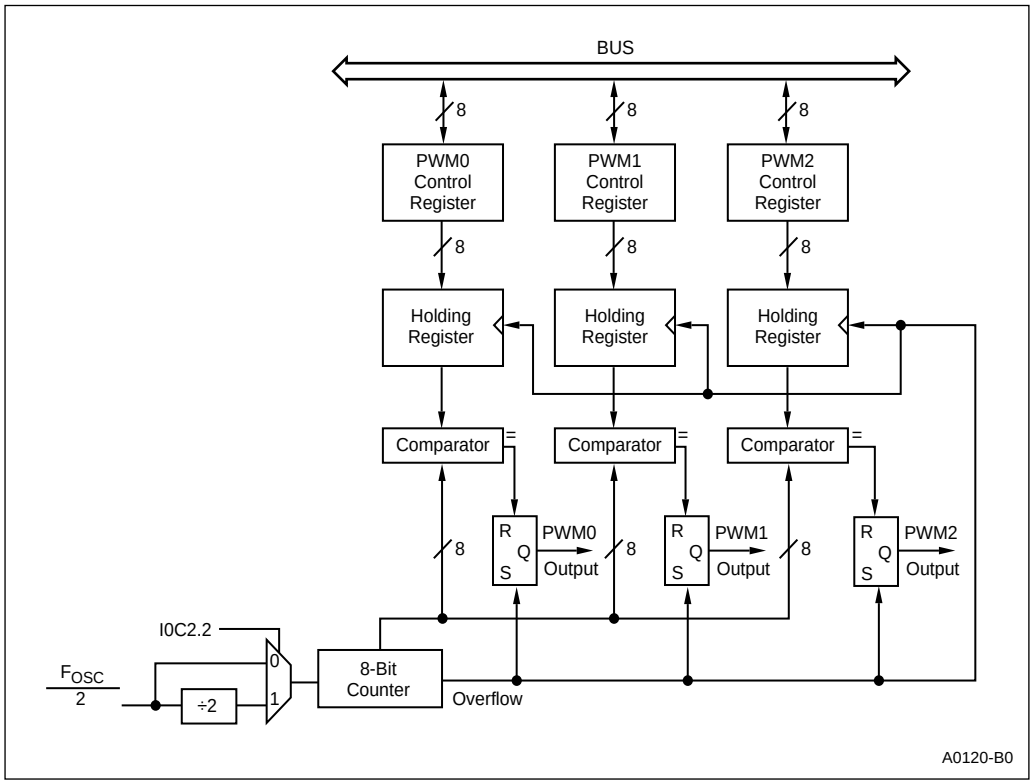

Figure 6. PWM Block Diagram

The PWM has three channels, each consisting of a comparator, a control register, a holding register, and an RS flip-flop. All three channels share an 8-bit counter and a divide-by-two clock prescaler. Each PWM channel can output a variable duty cycle pulse at a fixed frequency.

Apart from the difference in the number of output channels, the 8XC196KB and 8XC196KC PWM peripherals operate in the same manner. Each control register contains an 8-bit value that is loaded into a holding register when the 8-bit counter overflows. The comparators compare the contents of the holding registers to the counter value. When the counter value equals zero, then PWMx output channel is driven high. It will remain high until the counter value matches the value in the holding register, at which time the output is pulled low. When the counter overflows, the output is again switched high. Loading the PWMx_CONTROL register with the value 00H forces the output to remain low.

The PWMx_CONTROL register is used to determine how long the PWMx output is held high during the pulse, thus effectively controlling the duty cycle. The value written to PWMx_CONTROL register can be from 0 to 255 state times, which results in a duty cycle ranging from 0% to 99.6%. The formula used to calculate the PWM period and the time that the PWM output is high, with the clock prescaler disabled and enabled respectively; is shown below.

		Clock Prescaler Disabled (IOC2.2=0)	**Clock Prescaler Enabled (IOC2.2=1)**
T_{PWM} (in µs)	=	$\frac{512}{F_{OSC}}$	$\frac{1024}{F_{OSC}}$
Pulsewidth (in µs)	=	$\frac{PWMx\_CON \times 2}{F_{OSC}}$	$\frac{PWMx\_CON \times 4}{F_{OSC}}$

where:

PWM*x*_CON = 8-bit value to load into the PWM*x*_CONTROL register
F_{OSC} = the input frequency on XTAL1, in MHz

The SLOW_PWM (IOC2.2) bit controls the PWM output period by enabling or disabling the divide-by-two clock prescaler.

3.2 Timer 2 Differences

Both the 8XC196KB and 8XC196KC have two 16-bit timers, Timer 1 and Timer 2. Though Timer 1 is the same for these two microcontrollers, Timer 2 functions differently (see Table 6).

Table 6. Functional Attributes of Timer 2 on the 8XC196KB and 8XC196KC

8XC196KB's Timer 2	8XC196KC's Timer 2
Programmable 16-bit up/down counter	Programmable 16-bit up/down counter
External event capture	External event capture
Clocked externally using T2CLK or HSI.1	Clocked either **internally** or externally. Clocked externally using T2CLK or HSI.1
Fast Increment Mode: increments once every state time	Fast Increment Mode: increments once every state time
Normal Mode: increments once every eight state times	Normal Mode: increments once every eight state times

On the 8XC196KC, Timer 2 can be clocked either internally or externally. The external clocking scheme is similar to the 8XC196KB, in which either T2CLK or HSI.1 can be selected as the clock source. The internal clocking selection is controlled by the IOC3.0 bit (Timer 2 Internal Clock Enable). When this bit is set, the internal clock source is used. If the bit is clear, the external clock source is in control.

3.3 Standard and PTS Interrupts

Unlike the 8XC196KB, the 8XC196KC provides two interrupt service options: software interrupt service routines via the interrupt controller and microcoded hardware interrupt processing via the peripheral transaction server (PTS). The PTS services interrupts with less CPU overhead, does not modify the stack or the PSW, and allows normal instruction flow to continue. Also, the PTS can service an interrupt in the time required to execute a single instruction. Table 7 lists the vector locations for both software interrupt and PTS interrupt service routines.

Table 7. 8XC196KC Interrupt Vector Location

Interrupt Vector	Interrupt Vector Location	PTS Vector Location
HSI FIFO Full	203CH	205CH
EXTINT1	203AH	205AH
Timer 2 Overflow	2038H	2058H
Timer 2 Capture	2036H	2056H
HSI FIFO 4	2034H	2054H
Receive	2032H	2052H
Transmit	2030H	2050H
EXTINT	200EH	204EH
Serial Port	200CH	204CH
Software Timer	200AH	204AH
HSI.0	2008H	2048H
High Speed Output	2006H	2046H
HSI Data Available	2004H	2044H
A/D Conversion Complete	2002H	2042H
Timer Overflow	2000H	2040H

The PTS operates in five special microcoded modes that enable it to complete the specific tasks in much less time than a normal interrupt service routine. The five PTS modes are as follows:

- Single Transfer mode
- Block Transfer mode
- A/D Scan mode
- HSO mode
- HSI mode

Each PTS interrupt requires a block of data called the PTS Control Block (PTSCB). The PTSCB determines the PTS mode, the total number of PTS cycles, and the address of the source and destination of data transfers. The PTSCB for each interrupt source must be set up before enabling the PTS interrupt. Each PTSCB requires eight data bytes in register RAM, as shown in Figure 7.

Single Transfer	Block Transfer	A/D Scan Mode	HSO Mode	HSI Mode
—	—	—	—	—
—	PTSBLOCK	—	PTSBLOCK	PTSBLOCK
PTSDST (H)	PTSDST (H)	PTSREG (H)	—	—
PTSDST (L)	PTSDST (L)	PTSREG (L)	—	—
PTSSRC (H)	PTSSRC (H)	PTS_S/D (H)	PTSSRC (H)	PTSDST (H)
PTSSRC (L)	PTSSRC (L)	PTS_S/D (L)	PTSSRC (L)	PTSDST (L)
PTSCON	PTSCON	PTSCON	PTSCON	PTSCON
PTSCOUNT	PTSCOUNT	PTSCOUNT	PTSCOUNT	PTSCOUNT

Figure 7. PTS Control Blocks for 8XC196KC

As shown in Figure 7, the second location of each PTSCB is always the PTSCON register. The most significant three bits of the PTSCON register determine the PTS mode (see Figure 8).

PTSCON Address: PTSCB + 1

The PTS control (PTSCON) register selects the PTS mode and sets up control functions for that mode.

7							0
M2	M1	M0	†	†	†	†	†

Bit Number	Bit Mnemonic	Function
7:5	M2:0	PTS Mode These bits select the PTS mode: **M2 M1 M0** 0 0 0 single transfer 0 0 1 HSI mode 0 1 0 reserved 0 1 1 HSO mode 1 0 0 block transfer 1 0 1 reserved 1 1 0 A/D scan 1 1 1 reserved

† The function of this bit depends upon the mode selected. See the PTS control block description in each PTS mode section of your *8XC196KC/8XC196KD User's Manual*.

Figure 8. PTS Mode Selection Bits (PTSCON Bits 7:5)

After assigning an interrupt to the PTS, you must enable both the PTS interrupt globally and individually. The PTS Enable (PSE) bit in the Program Status Word (PSW) enables or disables the PTS globally. This is achieved by using the instruction EPTS to enable the PTS (set the PSE bit) and instruction DPTS to disable the PTS (clear the PSE bit). To individually enable or disable the PTS interrupt, set or clear the corresponding bit in the INT_MASK and INT_MASK1 register, respectively.

3.4 Slave Programming Differences

Among the three programming modes available on both 8XC196KB and 8XC196KC, auto programming mode, slave programming mode, and run-time programming mode; the slave programming mode is the only mode that does not function in the same manner on both controllers. The difference lies in the programming verification method.

On the 8XC196KB, when the data verify command is sent, the slave indicates the verification status of the previous data program command by driving one bit of ports 3 and 4. A "1" indicates a correct verification, and a "0" indicates an incorrect verification. The SID (slave identification) number of each slave determines which bit of ports 3 and 4 will be driven. For example, a SID of 0001 would drive port pin 3.1 to display the verification status of the slave programming.

On the 8XC196KC, the cumulative program verify (CPVER) function, multiplexed on P2.6, is used for verifying the slave programming status. This active-high output signal indicates whether any verify errors have occurred since the controller entered the programming mode. When the programming is completed, a "1" indicates that all locations have been programmed successfully. If an error occurred during the programming operation, then this signal will be driven to "0".